

REMARKS

Claims 1-2, 5-15, and 19-22 are pending in the application. Of these, claims 1, 15, and 20 are independent. Favorable reconsideration and examination are respectfully requested.

In the office action of April 17, 2006, claims 1-2, 5-8, 15, 19 and 20-22 were rejected under 35 U.S.C. 103(a) over Boyd et al (US 2002/0028555; hereinafter Boyd) in view of Thomas et al (US 2002/0019202; hereinafter Thomas). Claim 9 was rejected under 35 U.S.C. 103(a) over Boyd in view of Thomas and further in view of Buynoski (US 6,194,299; hereinafter Buynoski).

Examiner also indicated that claims 10-14 contain allowable subject matter and would be in condition for allowance if rewritten in independent form to include all the limitations of their base claims. Applicants, however, have not amended those claims, as suggested by the Examiner. Applicants believe that all of the claims, as presented, are allowable for at least the reasons set forth below.

In response to Applicants' reply to the Office Action of February 17, 2006, the Examiner indicated that the Applicants' arguments were unpersuasive. In particular, the Examiner appears to state that Boyd describes removing a silicide layer at a first rate and removing a polysilicon layer at a second rate (where the first rate is higher than the second rate). To provide this material, the Examiner appears to rely on Fig. 2D of Boyd appearing similar to a Fig. 12 in the subject application. Reciting from pages 9 and 10 of the subject action, the Examiner states:

On page 7 of the instant specification, the applicants discloses "Referring also to Fig. 12, chemical mechanical polishing is continued to remove cobalt silicide region 46 from a top surface of polysilicon gate electrode 18. The chemical mechanical polishing is performed with a slurry providing a relatively low polishing rate for chemical mechanical polysilicon 18, a relatively high for interlevel silicon dioxide 52, and a sufficiently high polishing rate for silicon nitride 50 and cobalt silicide 46 to achieve the structure illustrated in Fig. 12", Fig 12 shows that the gate polysilicon 18 is intact and the silicide 46 is completely removed after the CMP polishing step. Since Fig. 2D of Boyd also shows that the silicide 36 is completely removed while the polysilicon 52 remains intact after/as a result of the CMP polishing step, as similarly depicted in Fig. 12 of the instant specification, one skilled in the art would have found that it is obvious that Boyd silicide layer is removed at a higher rate than the polysilicon layer.

The Examiner appears to suggest that the claimed methodology used to produce the structure shown in Fig. 12 of the application is disclosed in Boyd by the mere illustration of a similar structure in Fig. 2D (of Boyd). While both figures may have similar structures, which is not conceded by the Applicants, Boyd neither discloses nor suggests removing a silicide layer at a first rate and removing a polysilicon layer at a second rate (where the first rate is higher than the second rate). Rather, Boyd describes implementing one technique for removing silicide region and another technique for removing a polysilicon layer. In this regard, Boyd recites:

[0072] After forming the insulator layer over the structure, any conventional planarization process such as chemical-mechanical polishing or grinding may be employed. It is noted that the planarization process employed in this step of the present invention is stopped after the silicide region 36 formed on top of polysilicon layer 52 is removed. Thus, the planarization exposes polysilicon layer 52 of the dummy gate region. The structure formed after conducting the above planarization step is shown in FIG. 2D.

[0073] Next, polysilicon layer 52 is removed utilizing RIE or a chemical down stream etching process exposing pad oxide layer 14. The exposed pad oxide is then etched utilizing the COR process mentioned above so that a taper is formed in the pad oxide layer, See FIG. 2E. The combined etch steps form opening 24 in the structure, wherein said opening contains a tapered pad oxide layer.

Boyd describes using a conventional planarization process such as chemical-mechanical polishing or grinding to remove the silicide region. Boyd then describes using reactive ion etching (RIE) or a chemical down stream etching process to remove the polysilicon layer. Thus, Boyd describes using one technique to remove silicide and another technique to remove polysilicon. In describing each technique, Boyd is silent in regards to disclosing or suggesting the rate at which the silicide and/or polysilicon is removed. Further, Boyd does not disclose or suggest that the rate at which the chemical-mechanical polishing (CMP) removes the silicide is higher than the rate at which the RIE or chemical etching process removes the polysilicon layer.

The Examiner appears to rely upon the MPEP as a basis to use Fig. 2D of Boyd to describe the removing a silicide layer at a first rate and removing a polysilicon layer at a second rate (where the first rate is higher than the second rate). The Examiner points out from MPEP section 2111 that pending claims must be given their broadest reasonable interpretation consistent with the specification (In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed.

Cir. 2000). The Applicants disagree with the Examiner's use of this passage to suggest that Boyd describes removing a silicide layer at a first rate and removing a polysilicon layer at a second rate (where the first rate is higher than the second rate). The Examiner appears to match a structure presented in the subject application with a structure presented in Boyd and use hindsight analysis to reject the methods of claims 1-2, 5-8, 15 and 19-22. Regarding hindsight analysis, the MPEP reads:

To reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the "differences," conduct the search and evaluate the "subject matter as a whole" of the invention. The tendency to resort to "hindsight" based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. (MPEP 2142 - Legal Concept of Prima Facie Obviousness)

The Examiner appears to improperly use hindsight to match Fig. 12 of the application with Fig. 2D of Boyd. But, even with this hindsight analysis, Boyd is silent in regards to disclosing or suggesting that the rate at which the chemical-mechanical polishing (CMP) removes the silicide is higher than the rate at which the RIE or chemical etching process removes the polysilicon layer. The structure depicted in Fig. 2D does not support the assertion that the silicide layer is removed at a higher rate than the polysilicon layer. There is no description in Boyd whatsoever that discloses or suggests that the rate of removal of the silicide layer is higher than the rate of removal of the polysilicon layer.

Thomas does not remedy the foregoing deficiencies of Boyd. In fact, the Examiner appears to concede that Thomas neither discloses nor suggests removing a silicide layer at a first rate and removing a polysilicon layer at a second rate (where the first rate is higher than the second rate). Reciting from page 10 of the Final Action:

In response, Thomas is relied upon to teach that it is desirable for the removal rate of each layer to differ significantly from each other during polishing, and is not relied upon to teach to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate where the first rate is higher than the second rate. The primary reference of Boyd suggests that the silicide layer is removed at a first rate and the polysilicon layer is removed at a second rate where the first rate is higher than the second rate.

Buynoski does not remedy the foregoing deficiencies of Boyd and Thomas with respect to independent claims 1, 15, and 20. Accordingly, for at least the foregoing reasons, claims 1, 15, and 20 are believed to distinguish over Boyd, Thomas and Buynoski individually and/or in combination.

Each of the dependent claims is also believed to define patentable features of the invention. Each dependent claim partakes of the novelty of its corresponding independent claim and, as such, has not been discussed specifically herein.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claims, except as specifically stated in this paper, and the amendment of any claims does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney can be reached at the address shown below. All telephone calls should be directed to the undersigned at 617-521-7896.

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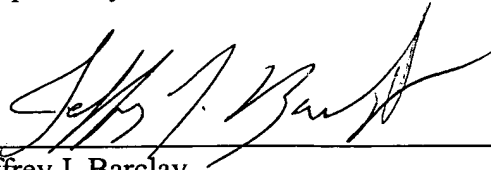
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Respectfully submitted,

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